This listing of claims will replace all prior versions, and listings, of claims in this application.

Listing of Claims

Claims 1-19 (cancelled)

20. (Previously Amended) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

first and second semiconductor chips each including a plurality of electrode pads, wherein the first semiconductor chip is bonded to a top surface of the chip attaching part and the second semiconductor chip is bonded to a bottom surface of the chip attaching part;

a package body encapsulating the semiconductor chips; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, wherein the inner leads having a second thickness, wherein the first thickness is smaller than the second thickness, wherein the peripheral part has a thickness equal to the second thickness of the inner leads, and wherein the peripheral part protrudes toward the second semiconductor chip.

21. (Original) An ultra-thin semiconductor package device according to claim 20, wherein the die pad is disposed below the leads.

22. (Previously Amended) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

first and second semiconductor chips each including a plurality of electrode pads, wherein the first semiconductor chip is bonded to a top surface of the chip attaching part and the second semiconductor chip is bonded to a bottom surface of the chip attaching part;

a package body encapsulating the semiconductor chips; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, wherein the inner leads having a second thickness, wherein the first thickness is smaller than the second thickness, wherein the peripheral part has a thickness equal to the second thickness of the inner leads, and wherein the bonding wires connected to one of the semiconductor chips are shorter than the bonding wires connected to the other semiconductor chip.

23. (Previously Amended) An ultra-thin semiconductor package device according to claim 20, wherein the bonding wires are connected by balls formed on the leads and stitches formed on the electrode pads.

24. (Original) An ultra-thin semiconductor package device according to claim 23, wherein metal bumps are formed on the electrode pads and wherein the stitches are formed on the metal bumps.

25. (Previously Amended) An ultra-thin semiconductor package device according to claim 20, wherein the die pad comprises divided first and second die pads.

26. (Original) An ultra-thin semiconductor package device according to claim 25, wherein the first and second die pads each include a corresponding chip attaching part and a corresponding peripheral part.

27. (Previously Amended) An ultra-thin semiconductor package device according to claim 20, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

28. (Previously Amended) An ultra-thin semiconductor package device according to claim 20, wherein a thickness of the package body is about 580 μm, a thickness of the die pad peripheral part is about 100 μm, and a thickness of the chip attaching part is about 40 μm.

29. (Previously Amended) An ultra-thin semiconductor package device according to claim 20, wherein an adhesive is attached to the backside of the chip in a wafer state to bond the semiconductor chips to the chip attaching part.

Claims 30-49 (withdrawn)

50. (Original) An electronic apparatus including a semiconductor package device having a package body of less than 0.7 mm of thickness, said semiconductor package device comprising:

a lead frame including a die pad, a plurality of leads disposed around the die pad, and a tie bar disposed around and connected to the die pad, wherein said die pad includes a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip having a plurality of electrode pads formed on an active surface of the chip, said chip connected to the chip attaching part;

a package body for encapsulating the semiconductor chip;

bonding wires encapsulated by the package body, said bonding wires configured to electrically connect the electrode pads of the semiconductor chip to the leads, wherein each of the plurality of leads comprises an inner lead bonded to the bonding wire and encapsulated by the package body and an outer lead integral to the inner leads and extending from the package body; and

wherein the chip attaching part has a first thickness and the inner lead has a second thickness that is greater than the first thickness.

51. (Original) An electronic apparatus according to claim 50, wherein the electronic apparatus is a memory card.

52. (Original) An electronic apparatus including a semiconductor package device having a package body of less than 0.7 mm of thickness, said semiconductor package device comprising:

a lead frame including a die pad, a plurality of leads disposed around the die pad, and a tie bar disposed around and connected to the die pad, said die pad including a chip attaching part and a peripheral part surrounding the chip attaching part, said peripheral part protruding away from the chip attaching part;

first and second semiconductor chips each having a plurality of electrode pads formed on an active surface of the chip, said first chip being attached to a top surface of the chip attaching part and the second chip being attached to a bottom surface of the chip attaching part;

a package body for encapsulating the semiconductor chip; and

bonding wires encapsulated by the package body and configured to electrically connect the electrode pads of the semiconductor chip and the plurality of leads, wherein each of the plurality of leads comprises an inner lead bonded to the bonding wire and encapsulated by the package body and an outer lead integral to the inner leads and extending from the package body, wherein said chip attaching part has a first thickness and the inner lead has a second thickness greater than the first thickness and equal to a thickness of the peripheral part.

53. (Original) An electronic apparatus according to claim 52, wherein the electronic apparatus is a memory card.

54. (Currently amended) The ultra-thin semiconductor package device according to claim ~~11~~ 52, further comprising another semiconductor chip attached to a back side of the chip attaching part.

55. (Previously added) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of leads disposed around the die pad, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the die pad chip attaching part, said chip having a plurality of electrode pads, wherein the plurality of electrode pads are electrically interconnected to the leads, and wherein each of the leads comprises integrally connected inner leads and outer leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and the inner leads having a constant second thickness greater than the first thickness, wherein the chip attaching part and the peripheral part have the same thickness.

56. (Previously added) The ultra-thin semiconductor package device according to claim 55, wherein the inner leads are formed of a single layer.

57. (Previously added) The ultra-thin semiconductor package device according to claim 55, wherein the first thickness is between about 30% to 50% of the second thickness.

58. (Previously added) The ultra-thin semiconductor package device according to claim 55, further comprising another semiconductor chip attached to a back side of the chip attaching part.

59. (Previously added) The ultra-thin semiconductor package device according to claim 55, wherein the die pad is located below the leads.

60. (Previously added) The ultra-thin semiconductor package according to claim 55, wherein the plurality of electrode pads are electrically interconnected to the leads via bonding wires, and wherein the bonding wires are connected by balls formed on the surface of the leads and stitches formed on the electrode pads.

61. (Previously added) The ultra-thin semiconductor package device according to claim 60, wherein metal bumps are formed on the electrode pads of the chip and the stitches are formed on the metal bumps.

62. (Previously added) The ultra-thin semiconductor package device according to claim 55, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

63. (Previously Added) The ultra-thin semiconductor package device according to claim 59, wherein the tie bar has the same thickness as the leads.

64. (Previously Added) The ultra-thin semiconductor package device according to claim 55, wherein the tie bar has the same thickness as the die pad peripheral part.

65. (Previously Added) The ultra-thin semiconductor package device according to claim 55, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads.

66. (Previously Added) The ultra-thin semiconductor package device according to claim 55, wherein the die pad comprises divided first and second die pads.

67. (Previously Added) The ultra-thin semiconductor package device according to claim 66, wherein the first and second die pads each include a chip attaching part and a peripheral part.

68. (Previously Added) The ultra-thin semiconductor package device according to claim 55, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

69. (Previously Added) The ultra-thin semiconductor package device according to claim 60, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

70. (Previously Added) The ultra-thin semiconductor package device according to claim 55, wherein the semiconductor chip is a memory device and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

71. (Previously Added) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of leads disposed around the die pad, wherein each of the plurality of leads comprises an inner lead and an outer lead, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the die pad chip attaching part, said chip having a plurality of electrode pads, wherein each of the plurality of electrode pads is electrically connected to at least one of the plurality of leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and a portion of the inner leads having a second thickness greater than the first thickness, wherein the bonding wires are connected to the portion of the inner leads, and wherein the chip attaching part and the peripheral part have the same thickness.

72. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the inner leads are formed of a single layer.

73. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the first thickness is between about 30% to 50% of the second thickness.

74. (Previously Added) The ultra-thin semiconductor package device according to claim 71, further comprising another semiconductor chip attached to a back side of the chip attaching part.

75. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the die pad is located below the leads.

76. (Previously Added) The ultra-thin semiconductor package according to claim 71, wherein the plurality of electrode pads are electrically interconnected to the leads via bonding wires, and wherein the bonding wires are connected by balls formed on the surface of the leads and stitches formed on the electrode pads.

77. (Previously Added) The ultra-thin semiconductor package device according to claim 76, wherein metal bumps are formed on the electrode pads of the chip and the stitches are formed on the metal bumps.

78. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

79. (Previously Added) The ultra-thin semiconductor package device according to claim 75, wherein the tie bar has the same thickness as the leads.

80. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the tie bar has the same thickness as the die pad peripheral part.

81. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads.

82. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the die pad comprises divided first and second die pads.

83. (Previously Added) The ultra-thin semiconductor package device according to claim 82, wherein the first and second die pads each include a chip attaching part and a peripheral part.

84. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

85. (Previously Added) The ultra-thin semiconductor package device according to claim 76, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

86. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the semiconductor chip is a memory device and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

87. (Previously Added) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and tie bars connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding the chip attaching part;

a first and a second semiconductor chip each including a plurality of electrode pads connected to the leads by bonding wires, wherein the first semiconductor chip is bonded to a top surface of the chip attaching part and the second semiconductor chip is bonded to a bottom surface of the chip attaching part; and

a package body encapsulating the first and the second semiconductor chips;

wherein said leads have a plurality of inner leads to which the bonding wires are bonded encapsulated within the package body, wherein said leads have a plurality of outer

leads exposed from the package body, wherein the plurality of inner leads have a second thickness that is greater than the first thickness, and wherein the bonding wires connected to one of the first and the second semiconductor chips are shorter than the bonding wires connected to the other one of the first and the second semiconductor chips.

88. (Previously Added) The ultra-thin semiconductor package device according to claim 87, wherein the peripheral part protrudes upwards and away from the chip attaching part, and wherein the bonding wires connected to an upper one of the first and the second semiconductor chips are shorter than the bonding wires connected to a lower one of the first and the second semiconductor chips.

89. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the inner leads are formed of a single layer.

90. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the first thickness is between about 30% to 50% of the second thickness.

91. (Previously Added) The ultra-thin semiconductor package according to claim 88, wherein the bonding wires are connected to the leads by balls formed on the surface of the leads and wherein the bonding wires are connected to the electrode pads by stitches formed on the electrode pads.

92. (Previously Added) The ultra-thin semiconductor package device according to claim 91, wherein a metal bump is formed on the electrode pads and the stitches are formed on the metal bumps.

93. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

94. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the tie bars have the same thickness as the leads.

95. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the tie bars have the same thickness as the peripheral part.

96. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the second thickness.

97. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the die pad comprises divided first and second die pads.

98. (Previously Added) The ultra-thin semiconductor package device according to claim 97, wherein the first and second die pads each include a chip attaching part and a peripheral part.

99. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein an adhesive bonds the first and the second semiconductor chips to the chip attaching part.

100. (Previously Added) The ultra-thin semiconductor package device according to claim 99, wherein the first and the second semiconductor chips are memory devices and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

101. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

102. (Previously Added) The ultra-thin semiconductor package device according to claim 87, wherein the peripheral part protrudes downwards and away from the chip attaching part, and wherein the bonding wires connected to a lower one of the first and the second semiconductor chips are shorter than the bonding wires connected to an upper one of the first and the second semiconductor chips.

103. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the inner leads are formed of a single layer.

104. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the first thickness is between about 30% to 50% of the second thickness.

105. (Previously Added) The ultra-thin semiconductor package according to claim 102, wherein the bonding wires are connected to the leads by balls formed on the surface of the leads and wherein the bonding wires are connected to the electrode pads by stitches formed on the electrode pads.

106. (Previously Added) The ultra-thin semiconductor package device according to claim 105, wherein a metal bump is formed on the electrode pads and the stitches are formed on the metal bumps.

107. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

108. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the tie bars have the same thickness as the leads.

109. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the tie bars have the same thickness as the peripheral part.

110. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the second thickness.

111. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the die pad comprises divided first and second die pads.

112. (Previously Added) The ultra-thin semiconductor package device according to claim 111, wherein the first and second die pads each include a chip attaching part and a peripheral part.

113. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein an adhesive bonds the first and the second semiconductor chips to the chip attaching part.

114. (Previously Added) The ultra-thin semiconductor package device according to claim 113, wherein the first and the second semiconductor chips are memory devices and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

115. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

116. (New) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of leads disposed around the die pad, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the die pad chip attaching part and another semiconductor chip mounted to another side of the chip attaching part, said semiconductor chip having a plurality of electrode pads, wherein the plurality of electrode pads are electrically interconnected to the leads, and wherein each of the leads comprises integrally connected inner leads and outer leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and the inner leads having a second thickness greater than the first thickness.

117. (New) An ultra-thin semiconductor package device according to claim 116, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads.

118. (New) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of leads disposed around the die pad, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a first semiconductor chip mounted to a first side of the chip attaching part and a second semiconductor chip mounted to a second side of the chip attaching part, said first and second chips having a plurality of electrode pads, wherein the plurality of electrode pads are electrically interconnected to the leads, and wherein each of the leads comprises integrally connected inner leads and outer leads;

an encapsulant encapsulating the first and second semiconductor chips to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and the inner leads having a constant second thickness greater than the first thickness, wherein the chip attaching part and the peripheral part have the same thickness.

119. (New) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of leads disposed around the die pad, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the die pad chip attaching part, said chip having a plurality of electrode pads, wherein the plurality of electrode pads are electrically interconnected to the leads, and wherein each of the leads comprises integrally connected inner leads and outer leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and the inner leads having a constant second thickness greater than the first thickness, wherein the chip attaching part and the peripheral part have the same thickness, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and wherein the thickness of the peripheral part is equal to the thickness of the leads.

120. (New) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of leads disposed around the die pad, wherein each of the plurality of leads comprises an inner lead and an outer lead, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the chip attaching part and another semiconductor chip attached to a back side of the chip attaching part, said chips having a plurality of electrode pads, wherein each of the plurality of electrode pads is electrically connected to at least one of the plurality of leads;

an encapsulant encapsulating the semiconductor chips to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and a portion of the inner leads having a second thickness greater than the first thickness, wherein the bonding wires are connected to the portion of the inner leads, and wherein the chip attaching part and the peripheral part have the same thickness.

121. (New) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of leads disposed around the die pad, wherein each of the plurality of leads comprises an inner lead and an outer lead, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the die pad chip attaching part, said chip having a plurality of electrode pads, wherein each of the plurality of electrode pads is electrically connected to at least one of the plurality of leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and a portion of the inner leads having a second thickness greater than the first thickness, wherein the bonding wires are connected to the portion of the inner leads, wherein the chip attaching part and the peripheral part have the same thickness, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and wherein the thickness of the peripheral part is equal to the thickness of the leads.